NANOMAGNETIC AND SPINTRONIC DEVICES FOR ENERGY-EFFICIENT MEMORY AND COMPUTING
In memory of my late great-uncle, N. Seshagiri, who inspired my career in science and technology

Jayasimha Atulasimha

In memory of my uncle, Dalumama

Supriyo Bandyopadhyay
NANOMAGNETIC AND SPINTRONIC DEVICES FOR ENERGY-EFFICIENT MEMORY AND COMPUTING

Edited by
Jayasimha Atulasimha and Supriyo Bandyopadhyay
Virginia Commonwealth University, US

WILEY
Contents

About the Editors and Acknowledgments xi
List of Contributors xiii
Foreword xvii
Preface xix

1  Introduction to Spintronic and Nanomagnetic Computing Devices
   Jayasimha Atulasimha and Supriyo Bandyopadhyay

1.1  Spintronic Devices 1
1.2  Nanomagnetic Devices 3
   1.2.1  Use of Spin Torque to Switch Nanomagnets 6
   1.2.2  Other Methodologies for Switching Nanomagnets 6
1.3  Thinking beyond Traditional Boolean Logic 7
   References 7

2  Potential Applications of all Electric Spin Valves Made of
   Asymmetrically Biased Quantum Point Contacts
   Nikhil Bhandari, Maitreya Dutta, James Charles, Junjun Wan,
   Marc Cahay, and S.T Herbert

2.1  Introduction 9
2.2  Quantum Point Contacts 11
2.3  Spin Orbit Coupling 14
   2.3.1  Rashba SOC (RSOC) 15
   2.3.2  Dresselhaus SOC (DSOC) 15
   2.3.3  Lateral Spin-Orbit Coupling (LSOC) 16
2.4  Importance of Spin Relaxation in 1D Channels 18
2.5  Observation of a 0.5 Conductance Plateau in Asymmetrically Biased
   QPCs in the Presence of LSOC 20
   2.5.1  Early Experimental Results Using InAs QPCs 20
   2.5.2  NEGF Conductance Calculations 20
   2.5.3  Spin Texture Associated with Conductance Anomalies in QPCs 23
2.5.4 Prospect for Generation of Spin Polarized Current at Higher Temperature 25
2.5.5 Observation of Other Anomalous Conductance Plateaus in an Asymmetrically Biased InAs/In_{0.52}Al_{0.48} as QPCs 26
2.6 Intrinsic Bistability near Conductance Anomalies 27
   2.6.1 Experimental Results 28
   2.6.2 NEGF Simulations 30
2.7 QPC Structures with Four In-plane SGs: Toward an All Electrical Spin Valve 43
   2.7.1 Preliminary Results on Four-gate QPCs 43
   2.7.2 Experiments 46
   2.7.3 Onset of Hysteresis and Negative Resistance Region 50
2.8 Future Work 56
2.9 Summary 58
Acknowledgments 60
References 60

3 Spin-Transistor Technology for Spintronics/CMOS Hybrid Logic Circuits and Systems 65
   Satoshi Sugahara, Yusuke Shuto, and Shuu’ichirou Yamamoto
   3.1 Spin-Transistor and Pseudo-Spin-Transistor 65
      3.1.1 Spin – MOSFET 66
      3.1.2 Pseudo-Spin-MOSFET 69
   3.2 Energy-Efficient Logic Applications of Spin-Transistors 72
      3.2.1 Power Gating with Nonvolatile Retention 73
      3.2.2 Nonvolatile Bistable Circuits 75
      3.2.3 Break-even Time 76
   3.3 Nonvolatile SRAM Technology 78
      3.3.1 Static Noise Margin of Nonvolatile SRAM 79
      3.3.2 Energy Performance of NV-SRAM 81
   3.4 Application of Nonvolatile Bistable Circuits for Memory Systems 86
      References 88

4 Spin Transfer Torque: A Multiscale Picture 91
   Yunkun Xie, Ivan Rungger, Kamaram Munira, Maria Stamenova, Stefano Sanvito, and Avik W. Ghosh
   4.1 Introduction 91
      4.1.1 Background 91
      4.1.2 STT Modeling: An Integrated Approach 93
   4.2 The Physics of Spin Transfer Torque 94
      4.2.1 Free-Electron Model for Magnetic Tunnel Junction 96
   4.3 First Principles Evaluation of TMR and STT 102
      4.3.1 The TMR Effect in the MgO Barrier 104
      4.3.2 Currents and Torques in NEGF 114
      4.3.3 First Principles Results on Spin Transfer Torque 116
   4.4 Magnetization Dynamics 119
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.4.1</td>
<td>Landau-Lifshitz-Gilbert Equation</td>
<td>119</td>
</tr>
<tr>
<td>4.4.2</td>
<td>Spin Torque Switching in Presence of Thermal Fluctuations</td>
<td>121</td>
</tr>
<tr>
<td>4.4.3</td>
<td>Including Thermal Fluctuations: Stochastic LLG vs Fokker Planck</td>
<td>122</td>
</tr>
<tr>
<td>4.5</td>
<td>Summary: Multiscaling from Atomic Structure to Error Rate</td>
<td>125</td>
</tr>
<tr>
<td></td>
<td>Acknowledgments</td>
<td>129</td>
</tr>
<tr>
<td></td>
<td>References</td>
<td>129</td>
</tr>
</tbody>
</table>

5 Magnetic Tunnel Junction Based Integrated Logics and Computational Circuits 133

5.1 Introduction 133
5.2 GMR Based Field Programmable Devices 134
5.3 MTJ Based Field Programmable Devices 136
5.3.1 MTJ Structure and TMR Ratio 136
5.3.2 MTJ Based Magneto-Logic 137
5.3.3 Utilization of STT in MTJ Based Magneto-Logic 144
5.4 Information Transformation between Gates 145
5.4.1 Direct Communication Using Charge Current 146
5.4.2 Magnetic Domain Walls for Information Transferring 148
5.5 MTJ Based Logic-in-Memory Devices 148
5.6 Magnetic Quantum Cellular Automata 149
5.6.1 Introduction and Background 149
5.6.2 Experimental Demonstrations 150
5.7 All-Spin Based Magnetic Logic 155
5.7.1 Nonlocal Lateral Spin Valve Background 155
5.7.2 Critical Parameters for Operation 155
5.7.3 Selected Review of Experimental Demonstrations 156
5.7.4 Applications to All-Spin Logic Devices 158
5.8 Summary 161
|         | Acknowledgment | 161  |
|         | References | 162  |

6 Magnetization Switching and Domain Wall Motion Due to Spin Orbit Torque 165

6.1 Introduction 165
6.2 Theory 166
6.2.1 Rashba Effect 168
6.2.2 Spin Hall Effect 169
6.3 Magnetic Switching Driven by Spin Orbit Torque 171
6.4 Domain Wall Motion Driven by Spin Orbit Torque 176
6.5 Applications of Spin Orbit Torque 184
6.6 Conclusion 186
|         | References | 186  |
7 Magnonic Logic Devices 189
Alexander Khitun and Alexander Kozhanov

7.1 Introduction 189
7.2 Magnonic Logic Devices 197
7.3 Spin Wave-Based Logic Gates and Architectures 206
7.4 Discussion and Summary 212
References 216

8 Strain Mediated Magnetolectric Memory 221
N. Tiercelin, Y. Dusch, S. Giordano, A. Klimov, V. Preobrazhensky, and P. Pernod

8.1 Introduction 221
8.2 Concept of Unequivocal Strain- or Stress-Switched Nanomagnetic Memory 223
8.2.1 Magnetic Configuration and Equilibrium Positions 223
8.2.2 Quasi-Static Stress-Mediated Switching 225
8.3 LLG Simulations – Macrospin Model 226
8.3.1 Landau-Lifshitz-Gilbert Equation and Effective Magnetic Field 226
8.3.2 Memory Parameters 227
8.3.3 Results of the Macrospin Model 228
8.4 LLG Simulations – Eshelby Approach 231
8.4.1 Geometry of the Memory Element 232
8.4.2 Coupling with the External Magnetic Field 233
8.4.3 Coupling with the External Electric Field and Elastic Stress 234
8.4.4 Static Behavior of the System 234
8.4.5 Dynamic Behavior of the System 235
8.5 Stochastic Error Analysis 238
8.5.1 Statistical Mechanics of Magnetization in a Single-Domain Particle 238
8.5.2 Switching Process within the Magnetolectric Memory 243
8.6 Preliminary Experimental Results 248
8.6.1 Piezoelectric Actuator with in-Plane Polarization 248
8.6.2 Ferroelectric Relaxors with out-of-Plane Polarization 249
8.6.3 Magnetoelastic Switching in a Magneto-Resistive Structure 250
8.7 Conclusions 250
Acknowledgments 252
References 253

9 Hybrid Spintronics-Straintronics 259
Ayan K. Biswas, Noel D’Souza, Supriyo Bandyopadhyay, and Jayasimha Atulasimha

9.1 Introduction 259
9.1.1 Nanomagnetic Memory and Logic Devices: The Problem of Energy Dissipation in the Clocking Circuit 260
9.1.2 Switching Nanomagnets with Strain Could Drastically Reduce Energy Dissipation: Hybrid Spintronics-Straintronics Overview 261
9.1.3 Landau Lifshitz Gilbert (LLG) Equation 263

9.2 Nanomagnetic Memory Switched with Strain
9.2.1 Complete Magnetization Reversal (180° Switching): Complex out-of-Plane Dynamics 265
9.2.2 Switching the Magnetization between Two Mutually Perpendicular Stable Orientations and Extension to Stable Orientations with Angular Separation >90° 268
9.2.3 Complete 180° Switching with Stress Alone 269
9.2.4 Mixed Mode Switching of Magnetization by 180°: Acoustically Assisted Spin Transfer Torque (STT) Switching for Nonvolatile Memory 273

9.3 Straintronic Clocking of Nanomagnetic Logic 276
9.3.1 Two-State Dipole Coupled Nanomagnetic Logic 276
9.3.2 Four-state Multiferroic Nanomagnetic Logic (NML) 279
9.3.3 Switching Error in Dipole Coupled Nanomagnetic Logic (NML) 283
9.3.4 Straintronic Nanomagnetic Logic Devices (NML) 284

9.4 Summary and Conclusions 286
References 286

10 Unconventional Nanocomputing with Physical Wave Interference Functions 291
Santosh Khasanvis, Mostafizur Rahman, Prasad Shabadi, and Csaba Andras Moritz

10.1 Overview 291
10.2 Spin Waves Physical Layer for WIF Implementation 293
10.2.1 Physical Fabric Components 295
10.3 Elementary WIF Operators for Logic 298
10.4 Binary WIF Logic Design 303
10.4.1 Binary WIF Full Adder 303
10.4.2 Parallel Counters 306
10.4.3 Benchmarking Binary WIF Circuits vs. CMOS 309
10.4.4 WIF Topology Exploration 310
10.5 Multivalued WIF Logic Design 311
10.5.1 Multivalued Operators and Implementation Using WIF 312
10.5.2 Multivalued Arithmetic Circuit Example: Quaternary Full Adder 316
10.5.3 Benchmarking of WIF Multivalued Circuits vs. Conventional CMOS 318
10.5.4 Input/Output Logic for Data Conversion between Binary and Radix-r Domains 319
10.6 Microprocessors with WIF: Opportunities and Challenges 320
10.7 Summary and Future Work 326
References 326

Index 329

A color plate section falls between pages 44 and 45
About the Editors and Acknowledgments

Jayasimha Atulasimha

Jayasimha Atulasimha is Qimonda Associate Professor of Mechanical and Nuclear Engineering with a courtesy appointment in Electrical and Computer Engineering at the Virginia Commonwealth University, where he directs the Magnetism, Magnetic Materials and Magnetic Devices (M3) laboratory. He has authored or coauthored over 60 scientific articles including more than 40 journal publications on magnetostrictive materials, magnetization dynamics, and nanomagnetic computing and has given several invited talks at conferences, workshops and universities in the USA and abroad on these topics. His research interests include nanomagnetism, spintronics, magnetostrictive materials and nanomagnet-based computing devices. He received the NSF CAREER Award for 2013–2018. He currently serves on the Technical Committees for Spintronics, IEEE Nanotechnology Council, ASME Adaptive Structures and Material Systems, Device Research Conference (DRC), and as a Focus Topic organizer for the APS topical group on magnetism (GMAG). He is a member of ASME, APS and an IEEE Senior Member.

Supriyo Bandyopadhyay

Supriyo Bandyopadhyay is Commonwealth Professor in the Department of Electrical and Computer Engineering in Virginia Commonwealth University, Richmond, Virginia, USA, where he directs the Quantum Device Laboratory. His research interests are in broad areas of nanotechnology and focus on spintronics, nanomagnetism, energy-efficient and noncharge-based computing paradigms, optical properties of nanostructures, and self-assembly based nanosynthesis. He is the author/coauthor of over 300 peer reviewed research publications and has given over 100 invited or keynote talks in conferences, workshops and colloquia across four continents. He currently serves as the Chair of the Technical Committee on Spintronics within the Nanotechnology Council of the Institute of Electrical and Electronics Engineers (IEEE) and in the past served as the Chair of the Technical Committee on Compound Semiconductor Devices within the Electron Device Society of IEEE. He has served as an IEEE Distinguished Lecturer and also as a Vice President of the IEEE Nanotechnology Council. He is the winner of the Distinguished Scholarship Award at Virginia Commonwealth University, which is the highest award given by the university for scholarship to one faculty member each year, and
also won the faculty research award, the faculty interdisciplinary research award and the faculty service award from the College of Engineering at University of Nebraska where he was employed prior to coming to Virginia Commonwealth University. He currently serves on the editorial boards of six international journals and served on the editorial boards of seven other journals in the past. Dr Bandyopadhyay is a Fellow of the Institute of Electrical and Electronics Engineers, American Physical Society, Institute of Physics, the Electrochemical Society and the American Association for the Advancement of Science.

Acknowledgments

This work was supported by the US National Science Foundation under grants ECCS-1124714 and CCF-1216614. Jayasimha Atulasimha would also like to acknowledge the NSF CAREER grant CCF-1253370.
List of Contributors

Nikhil Bhandari
Spintronics and Vacuum Nanoelectronics Laboratory
University of Cincinnati
Cincinnati, OH, USA

Debanjan Bhowmik
Department of Electrical Engineering and Computer Sciences
University of California Berkeley
Berkeley, CA, USA

Ayan K. Biswas
Department of Electrical and Computer Engineering
Virginia Commonwealth University
Richmond, VA, USA

Marc Cahay
Spintronics and Vacuum Nanoelectronics Laboratory
University of Cincinnati
Cincinnati, OH, USA;
Physics Department
University of Cincinnati
Cincinnati, OH, USA

James Charles
School of Electrical Engineering
Purdue University
West Lafayette, IN, USA

Noel D’Souza
Department of Mechanical and Nuclear Engineering
Virginia Commonwealth University
Richmond, VA, USA

Y. Dusch
LIA LICS/LEMAC, IEMN UMR CNRS 8520, Univ. Lille, Centrale Lille
Lille, France
Maitreya Dutta
Spintronics and Vacuum Nanoelectronics Laboratory
University of Cincinnati
Cincinnati, OH, USA

Avik W. Ghosh
Charles L Brown School of Electrical and Computer Engineering
University of Virginia
Charlottesville, VA, USA

S. Giordano
LIA LICS/LEMAC, IEMN UMR CNRS 8520, Univ. Lille, Centrale Lille
Lille, France

S.T. Herbert
Department of Physics
Xavier University
Cincinnati, OH, USA

Mahdi Jamali
University of Minnesota
Minneapolis, MN, USA

Santosh Khasanvis
University of Massachusetts Amherst
Amherst, MA, USA

Alexander Khitun
University of California
Riverside, CA, USA

A. Klimov
International Associated Laboratory LIA LEMAC
Lille, France;
Moscow Institute of Radio Engineering and Automation MIREA
Moscow, Russia;
V.A. Kotelnikov Institute of Radioengineering and Electronics
Moscow, Russia

Alexander Kozhanov
Georgia State University
Atlanta, GA, USA

OukJae Lee
Department of Electrical Engineering and Computer Sciences
University of California Berkeley
Berkeley, CA, USA
Csaba Andras Moritz
University of Massachusetts Amherst
Amherst, MA, USA

Kamaram Munira
Center for Materials for Information Technology
University of Alabama
Tuscaloosa, AL, USA

P. Pernod
LIA LICS/LEMAC, IEMN UMR CNRS 8520, Univ. Lille, Centrale Lille
Lille, France

V. Preobrazhensky
LIA LICS/LEMAC, IEMN UMR CNRS 8520, Univ. Lille, Centrale Lille
Lille, France;
A.M. Prokhorov General Physics Institute RAS
Moscow, Russia

Mostafizur Rahman
University of Massachusetts Amherst
Amherst, MA, USA

Ivan Rungger
School of Physics, AMBER and CRANN Institute
Trinity College
Dublin, Ireland

Sayeef Salahuddin
Department of Electrical Engineering and Computer Sciences
University of California Berkeley
Berkeley, CA, USA

Stefano Sanvito
Center for Materials for Information Technology
University of Alabama
Tuscaloosa, AL, USA

Prasad Shabadi
University of Massachusetts Amherst
Amherst, MA, USA
Marvell Semiconductors

Yusuke Shuto
Imaging Science and Engineering Laboratory
Tokyo Institute of Technology
4259 Nagatsuta, Midori-ku, Yokohama, Japan
Angeline Klemm Smith
University of Minnesota,
Minneapolis, MN, USA

Maria Stamenova
School of Physics, AMBER and CRANN Institute
Trinity College
Dublin, Ireland

Satoshi Sugahara
Imaging Science and Engineering Laboratory
Tokyo Institute of Technology
4259 Nagatsuta, Midori-ku, Yokohama, Japan

N. Tiercelin
LIA LICS/LEMAC, IEMN UMR CNRS 8520, Univ. Lille, Centrale Lille
Lille, France

Junjun Wan
Intel Corporation
Hillsboro, OR, USA

Jian-Ping Wang
University of Minnesota
Minneapolis, MN, USA

Yunkun Xie
Charles L Brown School of Electrical and Computer Engineering
University of Virginia
Charlottesville, VA, USA

Shuu’ichirou Yamamoto
Imaging Science and Engineering Laboratory
Tokyo Institute of Technology
4259 Nagatsuta, Midori-ku, Yokohama, Japan

Long You
Department of Electrical Engineering and Computer Sciences
University of California Berkeley
Berkeley, CA, USA

Zhengyang Zhao
University of Minnesota
Minneapolis, MN, USA
Foreword

When I started out on my career, CMOS technology had just begun its domination in electronics. Although there are major challenges in continued scaling, no other technology was expected to be able to compete with CMOS commercially in the near future. However, the research community had always been interested in looking beyond CMOS and searching for alternative technologies. I was very fortunate to be surrounded by wise mentors and brilliant colleagues, who ultimately convinced me it would be fun to be in the arena of “beyond CMOS technologies.” On many occasions I wished somebody had written a book summarizing the most promising developments, saving professionals and students the time and aggravation of sifting through a plethora of many approaches. The fact that Jayasimha Atulasimha and Supriyo Bandyopadhyay are doing just that, putting together a collection of the latest and most promising developments in spintronics, is going to benefit not only young students and researchers new to the field, but will also provide a convenient reference for experts and experienced researchers to build their discoveries upon.

The field of spintronics has enjoyed rapid progress during the last decade, mostly due to the major challenge of excessive power dissipation in further CMOS scaling, which threatens perhaps a complete halt to scaling in the near future. As any active researcher in this field will tell you, the race to be the first to discover novel devices far beyond CMOS applications is both exhilarating as well as exhausting. It is therefore with great pleasure and honor that I am writing this foreword to introduce you to this timely treatise on the latest developments in this field, edited by recognized experts as well as my friends and colleagues, Supriyo Bandyopadhyay and Jayasimha Atulasimha.

This new book delivers a summary of the latest developments in spintronics in a way that is pleasantly digestible for any graduate level student and beyond, aspiring to excel in this field.

Professor Kang L. Wang

Distinguished Professor and Raytheon Chair in Electrical Engineering
University of California, Los Angeles
Preface

The complementary metal-oxide semiconductor (CMOS) device technology has dominated electronics for the last 70 years. CMOS has been able to scale down at an incredible pace, predicted by the famed Moore’s law. However, it appears that further scaling of CMOS devices may encounter a roadblock by the end of the decade due to various issues, primarily among which is the rapid increase in heat dissipation as more and more devices are packed on to a chip with increasing densities.

There is also a strong need for computing devices that can operate with 2–3 orders of magnitude lower energy dissipation than current CMOS devices in embedded applications. Mobile and medical applications would prefer processors that would dissipate so little power that they can be run on energy harvested from the ambient without requiring a separate power source. If this comes to pass, it will open up myriad applications in wearable electronics, medical devices embedded to monitor the health of patients and sensor networks that monitor critical infrastructure such as buildings and bridges.

For these reasons, several new device concepts have been advanced as potential replacements for CMOS devices, or to complement CMOS devices for specific applications such as nonvolatile memory and logic, or to implement certain functionalities such as neuromorphic computing in a way better than CMOS devices can. They draw upon different physical mechanisms to elicit computational or signal processing activity. Among these different physical paradigms, spintronic and nanomagnetic devices form an important class both for the rich variety of physical phenomena on which these devices are based and the many different device concepts that they have spawned.

The editors hope that this book will provide the reader with a broad understanding of the key concepts behind spintronic and nanomagnetic devices as well as summarize the latest developments in this field. Questions and comments can be addressed to J. Atulasimha (jatulasimha@vcu.edu) and S. Bandyopadhyay (sbandy@vcu.edu).